RDK X5 Module

Thermal Design Guide

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
V1.0	2026-02-05	Initial release.

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1 Introduction

This document provides thermal design guidelines for the RDK X5 Module. Its purpose is to assist customers in developing reliable system-level thermal solutions by offering reference designs, simulation results, and design recommendations.

Notes to Customers:

- Customers are strongly advised to read and fully understand this Thermal Design Guide before system design.
- Customers are responsible for implementing a complete system-level thermal solution to ensure that all key components operate within their specified temperature limits. Adequate thermal margin should be considered based on the application environment.
- For application-specific questions or design reviews, please contact D-Robotics Field Application Engineers (FAEs).
- The appendix section includes tests conducted on different cooling solutions, serving as a reference for customers.

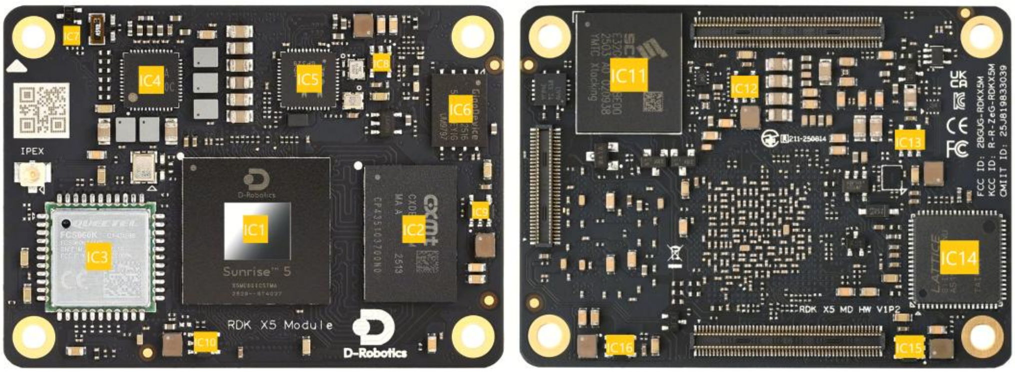
1.1 Definitions

Term	Description
SoC	System on Chip
T_J	Junction Temperature
T_A	Ambient temperature
R_{JB}	Junction-to-Board Thermal Resistance
R_{JC}	Junction-to-Case Thermal Resistance
TIM	Thermal Interface Material
MD	Module
CB	Carrier Board

2 Component Placement and Power Dissipation

2.1 Key Component Placement

The placement of key heat-generating components on the RDK X5 Module is illustrated in the figure below. These components should be considered primary thermal design targets during system integration.



2.2 Power Dissipation

Table below summarizes the reference thermal parameters and power dissipation values of the major components on the RDK X5 Module.

No.	Component	R_{JC} (℃/W)	R_{JB} (℃/W)	K Value (W/m·K)	T_J Spec. (℃)	Power Consumption (W)	Note
IC1	X5M	0.1	5.8		125	5@ T_J=85℃	3, 4
IC2	DRAM			4	T_C=85	0.4	2, 5
IC3	WIFI			4	T_A=80	1.5	2
IC4	PMIC	20.5	4.8		125	0.8	
IC5	Ethernet			4	125	0.28	2
IC6	Flash	15.5	15.5		125	0.06	
IC7	OVP			4	150	0.04	2
IC8	DCDC	27		4	125	0.1	2
IC9	DCDC	27		4	125	0.03	2
IC10	DCDC	27		4	125	0.1	2
IC11	EMMC	4.2		4	T_C=85	0.3	2, 5
IC12	DCDC	27		4	125	0.1	2
IC13	DCDC	27		4	125	0.02	2
IC14	HDMI	13.1		4	125	0.12	2
IC15	DCDC	27		4	125	0.1	2

No.	Component	R_{JC} (℃/W)	R_{JB} (℃/W)	K Value (W/m·K)	T_J Spec. (℃)	Power Consumption (W)	Note
IC16	DCDC	27		4	125	0.5	2

NOTE:

1. All parameters listed are reference values used for thermal simulation. Customers must verify actual power consumption and thermal characteristics in their specific applications.
2. For components, which do not show both R_{JC} and R_{JB} values in the table, it should be modeled as a single block with bulk thermal conductivity specified in the table.
3. The X5M is the key target in thermal design, and reliable cooling measures must be applied to it. In practical applications, the system software implements different performance and thermal control strategies based on the SOC junction temperature. T_J=125°C is the upper operating temperature limit of the device. Considering the accuracy of internal chip sensors and consistency deviations, it is recommended to set the simulation temperature upper limit target at T_J=120°C. During board operation, the temperature of this component must be monitored in real time to ensure the stable operation of the SOC.
4. The power consumption of the X5M is related to both the workload scenario and the chip junction temperature. It is recommended to set the simulation power consumption to the maximum value under the operating scenario. Specific values can be confirmed with D-robotics FAE.
5. As storage components, DRAM and eMMC are constrained by their case temperature (rather than junction temperature) in the design. The RDK X5 Module does not support reading the junction temperature or ambient temperature of these devices via temperature sensors. During the design verification phase, the temperature of these components must be tested using thermocouples to ensure that the design solution meets the intended targets.

3 Passive Cooling Reference Solution

Thermal simulations are performed to evaluate the feasibility of a system-level cooling solution under defined reference conditions. The results serve as a design reference to help customers assess thermal risks and optimize their own cooling solutions. This section introduces the design of the passive cooling solution.

3.1 Thermal Simulation Parameters

Simulation Environment

- Ambient temperature: 25°C.
- Cooling Condition: Natural convection, no forced airflow.
- If the customer's actual operating environment differs from the above conditions, it is strongly recommended to perform dedicated thermal simulations or measurements.

Heatsink Parameters

- Dimensions: 55mm x 40mm x 10mm
- Fin height: 8.7m
- Fin pitch: 5.57mm
- Fin thickness: 1mm
- Base plate thickness: 1.3mm

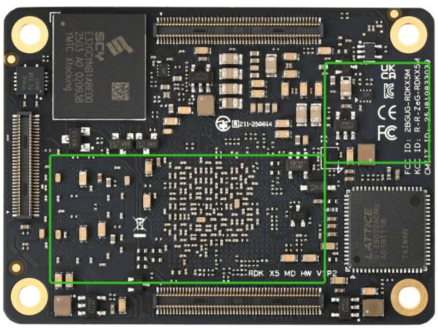
TIM

The properties of TIM are listed in table below.

No.	Location	Dimensions	Thermal Conductivity	Note
TIM1	X5M SoC	16*16*0.5mm	8W/m·K	
TIM2	DRAM	10*15*1.5mm	5W/m·K	
TIM3	PMIC	11*11*1.5mm	5W/m·K	
TIM4	Wi-Fi	11*11*1.5mm	5W/m·K	
TIM5	Between MD and CB	N/A	8W/m·K	1

NOTE:

1. TIM5 coverage area is indicated in the figure below.



Power Dissipation

Power dissipation values are referenced from Section 2.2 Power Dissipation of this document.

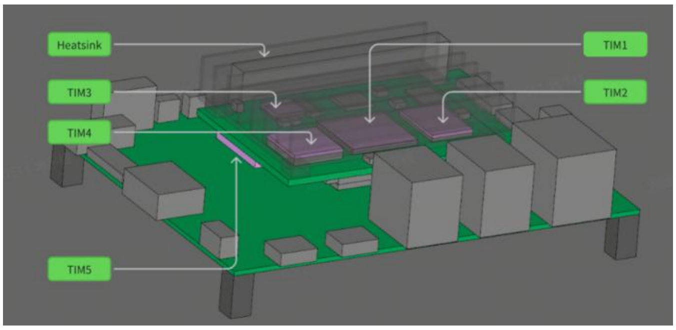
Material Properties

The thermophysical properties of materials are listed in table below.

Name	Material	Thermal Conductivity	Remark
Heatsink	AL6063-T5	180W/m·K	
PCB	FR4	K_X = K_Y = 20W/m·K K_Z = 4W/m·K	For reference only

3.2 Thermal Simulation Modeling

The modeled passive cooling configuration is shown in the figure below.



3.3 Simulation Temperatures of Key Components

Under a 25°C ambient temperature with natural convection and the specified passive cooling solution:

- The simulated temperature of the X5M SOC is 84.4°C, meeting the design objectives.
- All other components remain within their specified temperature limits with sufficient margin.

No.	Component	R_{JC} (℃/W)	R_{JB} (℃/W)	K Value (W/m·K)	T_J Target (℃)	Power Consumption (W)	Thermal Pedestal	Simulated Temperature T_J (℃)	Note
IC1	X5M	0.1	5.8		85	5	Yes	84.4	1
IC2	DDR			5	T_C=85	0.4	Yes	81.2	
IC3	WIFI			5	T_A=80	1.5	Yes	T_C=83.5	
IC4	PMIC	20.5	4.8		125	0.8	Yes	84.5	
IC5	Ethernet			5	125	0.28		82.4	
IC6	Flash	15.5	15.5		125	0.06		80.1	
IC7	OVP			5	150	0.04		80.9	
IC8	DCDC	27		5	125	0.1		84.5	
IC9	DCDC	27		5	125	0.03		78.1	
IC10	DCDC	27		5	125	0.1		79.5	
IC11	EMMC	4.2		5	T_C=85	0.3		T_C=80.1	

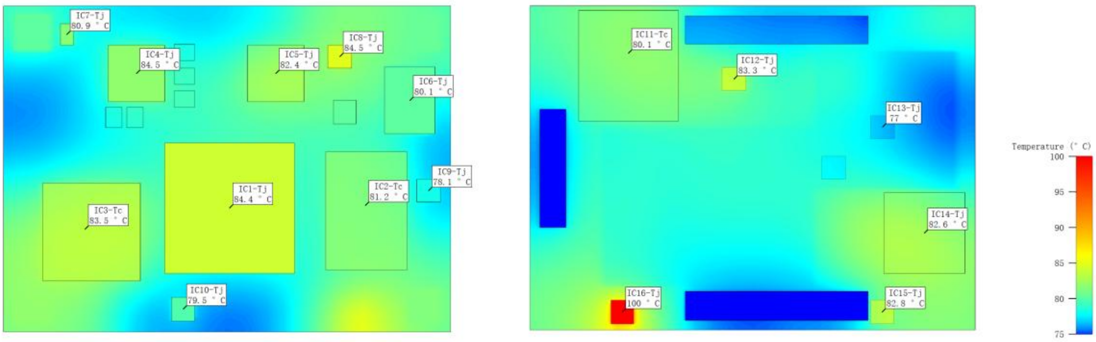
No.	Component	R_{JC} (℃/W)	R_{JB} (℃/W)	K Value (W/m·K)	T_J Target (℃)	Power Consumption (W)	Thermal Pedestal	Simulated Temperature T_J (℃)	Note
IC12	DCDC	27		5	125	0.1		83.3	
IC13	DCDC	27		5	125	0.02		77	
IC14	HDMI	13.1		5	125	0.12		82.6	
IC15	DCDC	27		5	125	0.1		82.8	
IC16	DCDC	27		5	125	0.5		100	

NOTE:

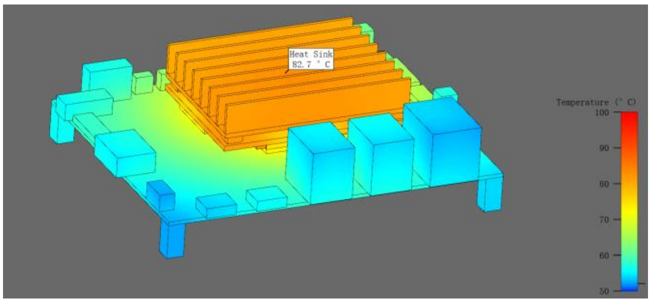
1. The 85 °C simulation target specified here is for demonstration purposes only. Customers should set their own limit target based on their specific requirements.

3.4 Simulation Contour Plot

PCB temperature distribution contour is shown below.



Heatsink temperature distribution contour is shown below.



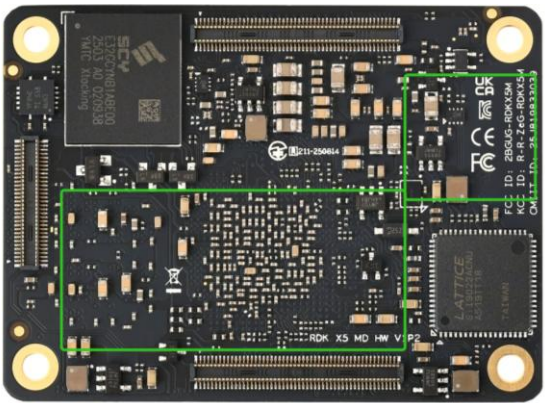
4 Design Conclusions and Recommendations

4.1 Design Conclusions

- The reference passive cooling solution maintains the X5M junction temperature below 85°C at a 25°C ambient temperature.
- This solution is suitable for room-temperature operation, such as development platforms, laboratory testing, or low-ambient commercial environments.
- For applications with higher ambient temperatures, restricted airflow, or sealed enclosures, customers should:
    1. Select a heatsink with improved thermal performance
    2. Use TIMs with higher thermal conductivity
    3. Consider active cooling solutions

4.2 General Design Recommendations

- The heatsink should ideally cover the entire module area to maximize heat spreading.
- Dedicated thermal paths should be implemented for X5M SoC, DRAM, and PMIC. Thermal mitigation for the Wi-Fi module is also recommended.
- Applying TIM between the MD and CB can further improve heat dissipation. The recommended TIM coverage area is indicated in the figure below. It is necessary to ensure that the TIM fully covers the designated area while avoiding any obstruction of the connectors.

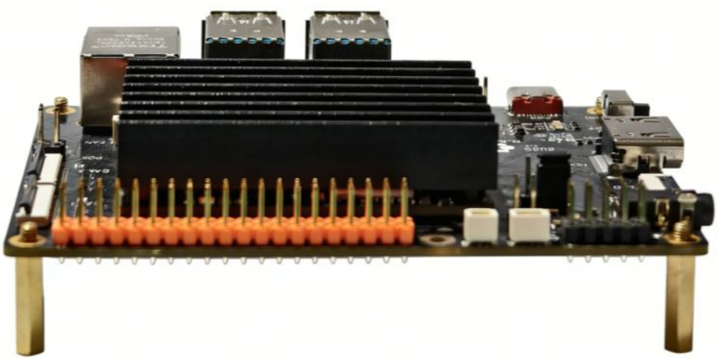


Appendix Verification Testing

This section includes verification tests conducted on two heatsink models to provide data for customer reference.

Appendix. A Passive Cooling

Based on the simulated thermal solution, a physical heatsink prototype was fabricated for validation testing.



Test Conditions

- Ambient Temperature: 38°C.
- Cooling Condition: Natural convection, no forced airflow.
- Test Scenario:
    1. 8x CPU @1.5GHz, 100% utilization
    2. 1x BPU @1.0GHz, 100% utilization
    3. LPDDR4 @4266MHz, 100% bandwidth utilization
    4. Dual camera input, load: 2x MIPI 1920*1080 @30fps, ISP+VSE+CODEC
    5. 3G GPU enabled
    6. DSP enabled

Test Results

The temperatures of the key components are as follows. The T_J of the X5M remains stable at 88.5 °C, which ensures stable system operation without triggering software-controlled thermal throttling (the default throttling temperature is 95 °C).

Component	Temperature(℃)	Note
T_A	38	1
X5M	T_J=88.5	2
DRAM	T_C=83.5	3
eMMC	T_C=84.4	3

NOTE:

1. In accordance with JESD51-2A, the ambient temperature thermocouple is placed 25 mm below the bottom plane of the test board.
2. The T_J of the X5M SOC is measured by an internal sensor and can be read via software.
3. The T_C of the DRAM and eMMC are measured using thermocouples.

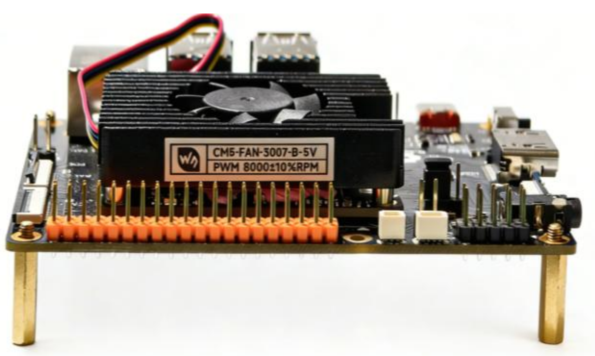
Appendix. B Active Cooling

When the ambient temperature exceeds 40°C, or when the system operates in a sealed or airflow-restricted enclosure, an active cooling solution is recommended. This can be achieved by replacing the passive heatsink with a fan-assisted heatsink assembly.

Tests were conducted on a common fan here.

Fan-heatsink Parameters

- Part Number: CM5-FAN-3007-B-5V
- Dimensions: 55mm x 40mm x 10mm
- Speed Control: PWM
- Rated Speed: 8000±10% PRM
- Power Supply: DC 5V



Test Conditions

- Ambient Temperature: 65°C

- Cooling Condition: Natural convection, no forced airflow
- PWM Duty Cycle: 100%
- Test Scenario:
  1. 8x CPU @1.5GHz, 100% utilization
  2. 1x BPU @1.0GHz, 100% utilization
  3. LPDDR4 @4266MHz, 100% bandwidth utilization
  4. Dual camera input, load: 2x MIPI 1920*1080 @30fps, ISP+VSE+CODEC
  5. 3G GPU enabled
  6. DSP enabled

Test Results

The temperatures of the key components are as follows. The T_J of the X5M remains stable at 84.4 °C, which ensures stable system operation without triggering software-controlled thermal throttling (the default throttling temperature is 95 °C).

Component	Temperature(℃)	Note
Ambient	65	
X5M	T_J=84.4	1
DRAM	T_C=73.6	2
EMMC	T_C=72.2	2

NOTE:

1. The T_J of the X5M SOC is measured by an internal sensor and can be read via software.
2. The T_C of the DRAM and eMMC are measured using thermocouples.